CLAIMS

1. An apparatus comprising:

an input section configured to generate a first control signal and a second control signal in response to an input signal and a select signal; and

an output section configured to generate an output signal in response to said first and second control signals, wherein said output signal is (i) related to said input signal when in a first mode and (ii) disabled when in a second mode.

2. The apparatus according to claim 1, wherein said apparatus comprises a push-pull multiplexer bit.

3. The apparatus according to claim 1, wherein an output load of said output signal is independent of an input load of said input signal.

4. The apparatus according to claim 3, wherein said output load is independent of said select signal.

5. The apparatus according to claim 1, wherein said first and second control signals are configured to eliminate output loading of said output signal from said input signal.

6. The apparatus according to claim 1, wherein coupling of non-selected inputs to said output signal is eliminated.

7. The apparatus according to claim 1, wherein said output signal comprises a complement of said input signal when in said first node.

8. A multiplexer or Programmable Interconnect Matrix comprising two or more of said apparatus of claim 1.

9. The apparatus according to claim 1, wherein said input section is further configured in response to said select signal and a complement of said select signal.

10. The apparatus according to claim 1, wherein said first and second modes are controlled by said first and second control signals.

11. The apparatus according to claim 1, wherein said input section comprises:

one or more first devices; and

one or more second devices coupled to said first devices and configured to generate said first and second control signals.

12. The apparatus according to claim 11, wherein:

said one or more first devices are coupled to said input signal and configured in response to said select signal; and

said one or more second devices are coupled to said select signal, a supply voltage, and a ground voltage.

13. The apparatus according to claim 12, wherein said output section comprises:

one or more third devices; and

one or more fourth devices, wherein said third and fourth devices are configured to present said output signal in response to said first and second control signals.

14. The apparatus according to claim 11, wherein said first mode comprises an enabled mode and said second mode comprises a disabled mode.

15. An apparatus comprising:

means for generating a first control signal and a second control signal in response to an input signal and a select signal; and

means for generating an output signal in response to said first and second control signals, wherein said output signal is (i) related to said input signal when in a first mode and (ii) disabled when in a second mode.

16. A method for tri-stating an output of a bit, comprising the steps of:

(A) generating a first state of said output by tracking an input when in a first mode;

(B) generating a second state of said output when in a second mode; and

(C) isolating said output from said input when in said second mode.

17. The method according to claim 16, wherein step (A) further comprises:

turning on one or more first devices; and

turning off one or more second devices.

18. The method according to claim 17, wherein step (B) further comprises:

turning on one or more third devices; and

turning off one or more fourth devices.

19. The method according to claim 16, wherein said first mode comprises an enabled mode and said second mode comprises a disabled mode.

20. The method according to claim 16, wherein said bit comprises a multiplexer bit.